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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/730,713	11/26/2003	Chen-Kuo Sun	79777	4010

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EXAMINER	
LU, TONY W	

ART UNIT	PAPER NUMBER
2878	

DATE MAILED: 05/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/730,713	SUN ET AL.	
	Examiner	Art Unit	
	Tony Lu	2878	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3 and 5-20* is/are pending in the application.

4a) Of the above claim(s) *2 and 4* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5-12 and 15-20* is/are rejected.

7)☒ Claim(s) *13 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is in response to the amendment filed on 1/30/2006.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1,3,5,7-10,15-18 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Sun et al US5239181.

With respect to claim 1, Sun et al disclose an optically clocked optoelectronic track and hold apparatus comprising:

a) a diode bridge(30) comprising a first node, a second node, a third node, a fourth node and a plurality of diodes, wherein said plurality of diodes comprises:

i) a first diode having a cathode operatively coupled to said first node and an anode operatively coupled to said second node;

ii) a second diode having a cathode operatively coupled to said third node and an anode operatively coupled to said first node;

iii) a third diode having a cathode operatively coupled to said fourth node and an anode operatively coupled to said second node;

iv) a fourth diode having a cathode operatively coupled to said third node and an anode operatively coupled to said fourth node;

b) an input node, operatively coupled to said first node of said diode bridge, capable of receiving an analog input signal(please refer to fig.2);

c) a first current source(V+ or S_2), operatively coupled to said second node of said diode bridge and a second current source(V- or S_1), operatively coupled to said third node of said diode bridge, and wherein said first and second current sources are capable of forward biasing said diode bridges(col.5);

d) a first photodetector(S_3) having a cathode operatively coupled to said second node and an anode operatively coupled to a negative potential node(V-) and a second photodetector(S_4) having an anode operatively coupled to said third node and a cathode operatively coupled to a positive potential node(V+), and wherein said first and second photodetectors are capable of receiving an optical input clocking signal(from laser 21), and capable of reverse biasing and forward biasing said diode bridge in response to said optical input clocking signal(col.4-5);

e) a hold capacitor(40), operatively coupled to said fourth node, capable of tracking said analog input signal when said diode bridge is forward biased, and capable of holding said analog input signal when said diode bridge switches from forward biased to reverse biased(col.4-5).

With respect to claim 3, per the above discussion, Sun et al disclose said at least two photodetectors are reverse biased by voltage sources(col.4-5).

With respect to claim 5, per the above discussion, Sun et al disclose said optical input clocking signal comprises a first optical input clocking signal(from fiber 22) and a second optical input clocking signal(from fiber 25), wherein a first photodetector(S_3) is

capable of receiving said first optical input clocking signal, and wherein a second photodetector(S_4) is capable of receiving said second optical input clocking signal, and wherein said first optical input clocking signal and said second optical input clocking signal are synchronized(col.5).

With respect to claim 7, per the above discussion, Sun et al disclose said first and second photodetectors switches said diode bridge from forward biased to reverse biased when said optical input clocking signal illuminates said first and second photodetectors with an optical pulse(col.4-5).

With respect to claim 8, per the above discussion, Sun et al disclose said first and second photodetectors switches said diode bridge from reverse biased to forward biased when said first and second photodetectors do not generate enough photocurrent to reverse bias said diode bridge(col.4-5).

With respect to claim 9, per the above discussion, Sun et al disclose said optically clocked optoelectronic track and hold apparatus having a positive node device(V+) and a negative node deivce(V-), wherein said optically clocked optoelectronic track and hold apparatus receives said analog input and output an output signal different from the analog input signal.

With respect to claim 10, per the above discussion, Sun et al disclose said optically clocked optoelectronic track and hold apparatus further comprises an amplifier(35), operatively coupled to said hold capacitor, capable of outputting a first track and hold output signal.

Sun et al's apparatus inherently performs the claimed method steps of claims 15-18 as it discloses all the limitations set forth above.

With respect to claim 20, Sun et al disclose an optically clocked optoelectronic track and hold apparatus comprising: means(a first node) for receiving an analog input signal and an optical input clocking signal(from the laser,21); means(diode bridge 30) for determining whether an optical pulse is received by at least two photodetectors from said optical input clocking signal; means(S_1-S_4) for maintaining a diode bridge(30) in forward bias if said optical pulse is not received from said optical input clocking signal; means(S_1-S_4) for switching said diode bridge to reverse bias for a desired time if said optical pulse is received from said optical input clocking signal.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sun et al US5239181 in view of MacDonald et al US4727349.

With respect to claim 6, per the above discussion, Sun et al lack a clear inclusion whether or not the photodetectors have fast rise time and long fall times.

MacDonald et al disclose a detector shows a fast rise time and long fall time(read col.1, lines 35-53).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Sun et al by utilizing photodetectors having fast rise times and long fall times taught by MacDonald et al in order to provide desired performances of the photodetectors.

The proposed system of Sun et al, discussed above, inherently performs the claimed method steps of claim 19 as it discloses all the limitations set forth above.

Claim 11 is rejected under 35 U.S.C 103(a) as being unpatentable over Sun et al US5239181 in view of Taddiken US5455584.

With respect to claim 11, per the above discussion, Sun et al fall to teach a quantizer capable of quantizing said first track and hold output signal and outputting a digital output signal.

Taddiken disclose high frequency high resolution quantizer having a quantizer(20), operatively coupled to a amplifier(16), capable of quantizing a track and hold output signal and outputting a digital output signal.

Although Sun et al lack a clear teaching of a quantizer, using a known and available quantizer in order to convert an analog input signal to a digital output signal would have been obvious to one of ordinary skill in the art.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Sun et al with a quantizer taught by Taddiken in order to provide a desired formation of the output signal.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sun et al US5239181 in view of Taddiken US5455584 as applied to claim 11 above, and further in view of Metz US4659945.

With respect to claim 12, per the above discussion, Sun et al and Taddiken fail teach a second electronic track and hold device, operatively coupled to said optically clocked optoelectronic track and hold apparatus, capable of receiving said first track and hold output signal and an electronic clock signal, wherein said electronic track and hold device is capable of outputting a second track and hold output signal.

Metz discloses a sampling bridge(see fig.7) with a first electronic track and hold device(12) and a second electronic track and hold device(20) being connected together, wherein the second electronic track and hold device(20) is capable of receiving a first track and hold output signal(from the first track and hold device), an electronic clock signal(IS1 and IS2) and outputting a second track and hold output signal(V_{out}).

Although Sun et al and Taddiken fail to teach an additional electronic track and hold device, operatively coupled to said optically clocked optoelectronic track and hold apparatus, capable of receiving said first track and hold output signal and an electronic clock signal, wherein said electronic track and hold device is capable of outputting a second track and hold output signal, utilizing an additional electronic track and hold device in order to provide compensation of the track and hold output signal from said optically clocked optoelectronic track and hold apparatus would have been obvious to one of ordinary skill in the art.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the proposed apparatus of Sun et al and Taddiken by supplying a second electronic track and hold device taught by Metz in order to provide a desired compensation to the output signal from the previous circuitry of the apparatus. This would provide a more reliable output signal from the apparatus.

Allowable Subject Matter

Claims 13 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art fails to disclose an optically clocked optoelectronic track and hold apparatus, among other features, comprises: one of first and second photodetectors is comprised of a short transit time photodiode and a long transit time photodiode in a parallel configuration.

Response to Arguments

Applicant's arguments filed 1/30/2006 have been fully considered but they are not persuasive.

With respect to applicant's argument, on page numbers 11-15 of the remarks, argues that the Sun et al (R1) includes a photodetecor configuration opposite of the present invention as defined in Claim 1. This statement is found not persuasive. Sun et

al(R1) disclose a first photodetector(S_3) having a cathode operatively coupled to said second node and an anode operatively coupled to a negative potential node(V-) and a second photodetector(S_4) having an anode operatively coupled to said third node and a cathode operatively coupled to a positive potential node(V+); a first current source(V+ or S_2), operatively coupled to said second node of said diode bridge and a second current source(V- or S_1), operatively coupled to said third node of said diode bridge(see fig.2), wherein the apparatus of Sun et al operates normally in track mode when the photodetectors(S_3, S_4) are not illuminated and operates in hold mode when the photodetectors are illuminated(see col.5, lines 1-35). Thus Suns et al operates as the claimed present invention.

Accordingly, the rejections set forth above are proper.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1) Benson US3721829 discloses a diode bridge sampling system, comprises two currents, two photodetectors and four photodiodes(see fig.2), operates to perform sample and hold function.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tony Lu whose telephone number is 5712728448. The examiner can normally be reached on M-F 9:00am- 6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Georgia Epps can be reached on 5712722328. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TL

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